



AMIRIX Email Trigger Core: Automatic Email Message Delivery

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Product Specification



SIGNONCE
IP LICENSE

AMIRIX Systems Inc.

77 Chain Lake Drive
Halifax, Nova Scotia
Canada, B3S 1E1
Phone: (902) 450-1700
Fax: (902) 450-1704
URL: www.amirix.com

Features

- ▶ Available under terms of the SignOnce IP License
- ▶ Self-contained block generates standard SMTP e-mail messages over IP/Ethernet
 - External 10/100 generic PHY interface
 - Protocol stack includes DNS and ARP
- ▶ Triggered by user H/W signal
 - Up to 64 signals sampled at trigger, and reported in e-mail message
- ▶ Included in standard ISE design flow. No software modifications or tools required.

Applications

- ▶ Event logging
- ▶ Remote monitoring
- ▶ Debugging

| AllianceCORE™ Facts | |
|---------------------------------------|---|
| Provided with Core | |
| Documentation | User Guide (README) |
| Design File Formats | Netlist with wrapper plus UCF |
| Constraints Files | UCF |
| Verification | Hardware (using AMIRIX's PCI Platform FPGA Development Board and Memec's V-II Pro P7-FG456 Board) |
| Instantiation templates | Verilog and VHDL |
| Reference designs & application notes | Simple reference design included |
| Additional Items | None |
| Simulation Tool Used | |
| ModelTech's Modelsim, Synopsys' VSS | |
| Support | |
| Support provided by AMIRIX Systems | |

General Description

The Email Trigger core offers a simple way to have programmable logic hardware send messages through the Internet, for remote monitoring or debugging. The Email Trigger is entirely self-contained, and uses a Virtex-II Pro embedded PowerPC. The interface to user hardware is very simple, and the only external requirement is for an Ethernet PHY. (A reference schematic is provided.)

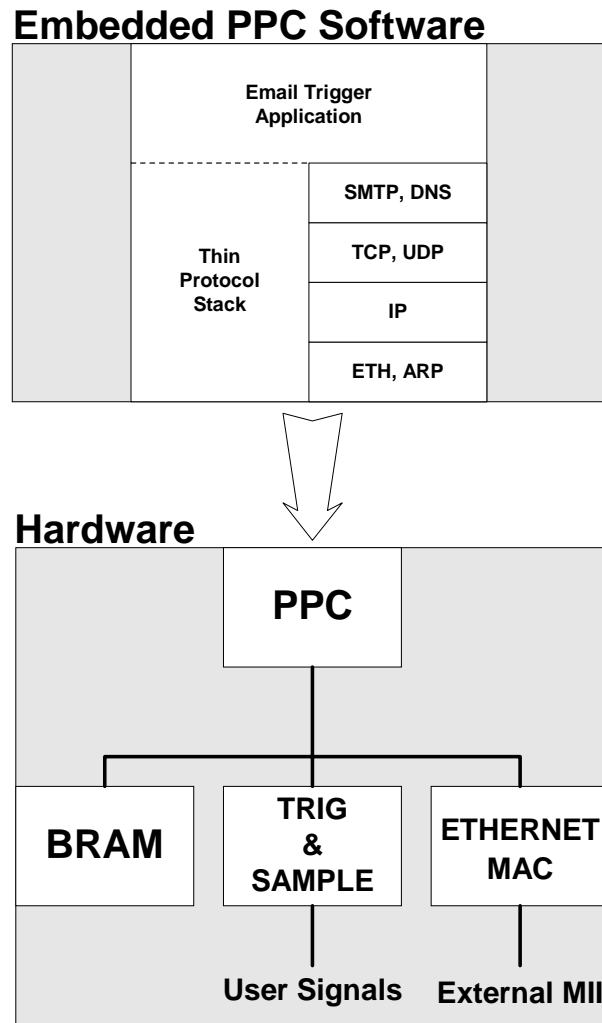
Table 1: Example Implementation Statistics

| Family | Example Device | Fmax (MHz) | Slices ¹ | IOB ² | GCLK | BRAM | MULT | DCM | MGT | PPC | Design Tools |
|---------------|----------------|------------|---------------------|------------------|------|------|------|-----|-----|-----|--------------|
| Virtex-II Pro | XC2VPxx-x | 100 | 2200 | 94 | 1 | 19 | 0 | 0 | 0 | 1 | ISE 5.2i |

Notes:

1. Actual slice count may vary depending on percentage of unrelated logic – see Mapping Report File for details
2. Assuming all core I/Os are routed off-chip

Figure 1: Email Trigger Block Diagram



Functional Description

Trigger/Sampler: On the rising edge of the Trigger signal, the Sample signals are latched and a register bit is set. The latched Sample values and the Trigger Bit are accessible through a CoreConnect interface. The Trigger Bit must be cleared via CoreConnect to restart the sequence.

Ethernet MAC: AMIRIX-proprietary 10/100/1000 Ethernet MAC with GMII interface.

RAM: Code and data storage for the CPU, implemented with Block RAM.

CPU: Virtex-II Pro embedded PPC405.

Software: Standalone application which at the top level polls the Trigger Bit, and composes and initiates e-mail messages. E-mail messages are delivered through an SNMP/TCP/IP stack, using DNS, ARP and a generic PHY interface. *(This product includes software developed by Adam Dunkels.)*

Core Modifications

Mandatory User Settings: The network parameters described in Table 2 must be set by the user. A script is provided to automatically patch these parameters into the UCF file.

Basic modifications available with source code:

- ▶ More complex triggering scenarios, and multiple messages
- ▶ Customized message content and format

Table 2: Network Parameters

| Parameter | Description | Example |
|----------------|---|------------------------------------|
| UIP_ETHADDR | Ethernet MAC address of the Email Trigger | 00:01:02:03:04:05 |
| UIP_IPADDR | IP address of the Email Trigger | 192.75.167.130 |
| UIP_NETMASK | Netmask | 255.255.255.0 |
| UIP_DRIPADDR | Default router IP address | 192.75.167.1 |
| UIP_DNSIPADDR | DNS server IP address | 192.75.167.14 |
| TRIG_SMTPSERV | DNS name of the SMTP server | smtp.amirix.com |
| TRIG_LOCALHOST | DNS name of the Email Trigger | trigger.amirix.com |
| TRIG_SENDTO | Email address to send message to | monitor@AMIRIX.com |
| TRIG_SENDFROM | Email address messages will appear to be from | trigger@AMIRIX.com |
| TRIG_SUBJECT | Subject line on email message | "AMIRIX Email Trigger" |
| TRIG_MESSAGE | Text of email message | "AMIRIX Email Trigger\n\nData %\n" |

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 3.

Verification Methods

The Email Trigger was verified in actual hardware using AMIRIX's PCI Platform FPGA Development Board and the Memec Virtex-II Pro P7-FG456 board.

Recommended Design Experience

Any designer with a basic understanding of the ISE design flow can include the Email Trigger in a design. Some assistance may be needed in setting network parameters, and Ethernet PHY support on the target hardware is required.

Ordering Information

This AllianceCORE product is available from Xilinx AllianceCORE member AMIRIX Systems under the terms of the SignOnce IP License. To learn about the SignOnce

IP License program, contact AMIRIX Systems, visit www.xilinx.com/ipcenter/signonce.htm or write to commonlicense@xilinx.com. Please contact AMIRIX Systems for pricing and additional information about this AllianceCORE product.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For AllianceCORE™ specific information, visit URL:

www.xilinx.com/products/logiccore/alliance/tblpart.htm

Table 3: Core I/O Signals

| Signal | Signal Direction | Description |
|----------------------|------------------|--|
| trigger_trigger | Input | Rising edge latches the value of the <i>Sample</i> signal, and initiates e-mail message. |
| trigger_sample(63:0) | Input | Values are latched upon trigger, and can be reported in the e-mail message |
| MAC_tx_clk | Input | MII Transmit Clock |
| MAC_tx_d(3:0) | Output | MII Transmit Data |
| MAC_tx_en | Output | MII Transmit Enable |
| MAC_tx_er | Output | MII Transmit Error |
| MAC_tx_led_n | Output | MII Transmit LED |
| MAC_rx_clk | Input | MII Receive Clock |
| MAC_rx_d(3:0) | Input | MII Receive Data |
| MAC_rx_dv | Input | MII Receive Data Valid |
| MAC_rx_er | Input | MII Receive Error |
| MAC_rx_led_n | Output | MII Receive LED |
| MAC_crs | Input | MII Carrier Sense |
| MAC_col | Input | MII Collision |
| MAC_mdc | Output | MDIO Clock |
| MAC_mdio_I | Input | MDIO Data Input |
| MAC_mdio_O | Output | MDIO Data Output |
| MAC_mdio_T | Enable | MDIO Output Enable |
| MAC_phy_resetrn | Output | Reset for external Ethernet PHY |
| system_reset | Input | Email Trigger Reset |
| sys_clk | Input | CoreConnect Bus Clock |
| HALTNEG | Input | PPC405 JTAG Port: Useful for debugging, but not needed during normal deployment. (HALTNEG inverted to drive dbg405debughalt) |
| jtgc405tck | Input | |
| jtgc405tdi | Input | |
| c405jtgtdo | Output | |
| jtgc405trstneg | Input | |
| jtgc405tms | Input | |