

# Gigabit Ethernet Core

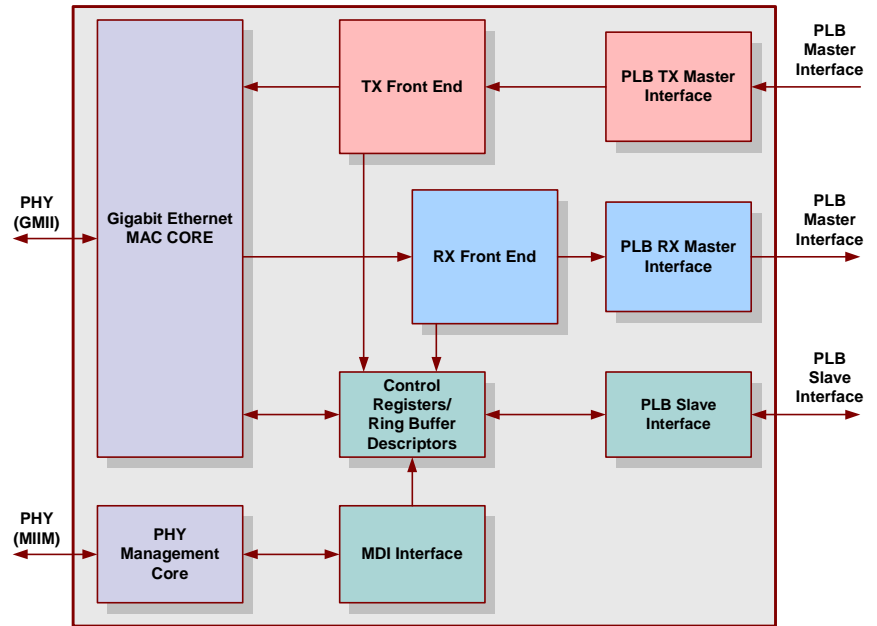
The AMIRIX Gigabit Ethernet Core is an interface core that lies between a PHY device and a CoreConnect Processor Local Bus (PLB). It is optimized for use in a processor based system and uses Direct Memory Access (DMA) for improved performance. All registers and buffer descriptors are memory mapped and can be accessed directly over the Processor Local Bus. PHY management functions are included. See the adjacent block diagram for a more complete description.

## Features

- ▶ IEEE 802.3-2000 compliant Gigabit Ethernet MAC
- ▶ Targeted to Xilinx Virtex-II Pro™ devices
- ▶ 1000 Mb/s, full duplex
- ▶ Supports Jumbo frames (up to 9180 bytes)
- ▶ Optional FCS (CRC-32) generation and checking
- ▶ Error reporting
- ▶ Detects VLAN tagged frames
- ▶ GMIIM interface to external PHY device
- ▶ PHY Management Interface (MIIM)
- ▶ Separate 64-bit PLB master interfaces for transmit and receive DMA engines using 32-byte burst accesses
- ▶ PLB slave interface for access to Control Registers and Ring Buffer Descriptors
- ▶ Up to 256 transmit and 256 receive Ring Buffer Descriptors stored in BlockRAM within the core
- ▶ Counts Lost Packets, FCS Errors, and Pause Frame Errors (16 bits with rollover indication)
- ▶ Optional continuous mode (re-uses buffer descriptors)
- ▶ Receive and Transmit packet interrupts
- ▶ Programmable receive packet interrupt hold-off
- ▶ 16 KB Transmit and Receive FIFOs
- ▶ Third Party PHYs used to date:
  - Marvell 10/100/1000 Ethernet Transceiver, Part #88e1011-BAB
  - National Semiconductor 10/100/1000 Ethernet Physical Layer, Part #DP83865-BHV

## Deliverables

- ▶ Source (Verilog RTL), Netlist, or Evaluation Netlist
- ▶ Packaged as a Xilinx Embedded Development Kit (EDK) User Core and can also be used outside of EDK
- ▶ Sample UCF, instantiation template and clock module
- ▶ Linux Driver Source: can be compiled as a loadable module or as part of the kernel
- ▶ Users Guide



## Verification

- ▶ Verified in hardware using the AMIRIX AP100 family

## Core Statistics

Target Devices	
Xilinx FPGA	Virtex-II™, Virtex-II Pro™
Resource Usage	
Slices (approximate)	1706
Flip Flops	1157
Lookup Tables	2997
BlockRAM	23
I/O	28

Note: Requires 2 global clock buffers instantiated outside of core. One for the transmit clock (can be shared with multiple instances of the same core), and one for the receive clock. No DCM required.



AMIRIX is a member of the Xilinx Alliance Program.



## Ordering Information

**License Formats Available:** Gigabit Ethernet Core Evaluation  
 Gigabit Ethernet Core Netlist  
 Gigabit Ethernet Core Source (Verilog)

## Contact

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